FIG. 1

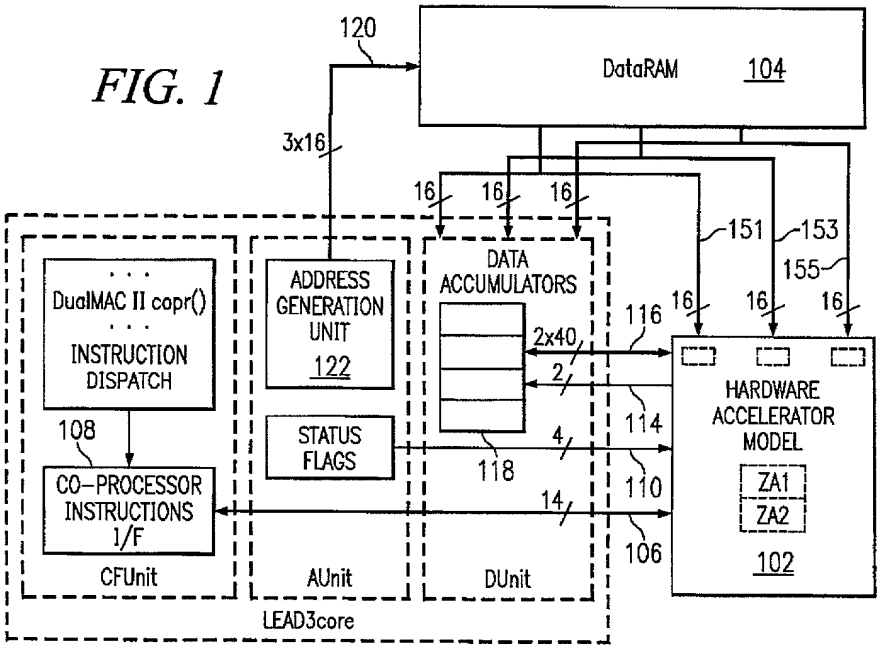

120
DataRAM
104
3x16
16
16
16
151
153
155
DUalMAC II copr()
INSTRUCTION
DISPATCH
ADDRESS
GENERATION
UNIT
122
DATA
ACCUMULATORS
116
16
16
16
2x40
2
HARDWARE
ACCELERATOR
MODEL
ZA1
ZA2
102
114
108
STATUS
FLAGS
4
118
110
CO-PROCESSOR
INSTRUCTIONS
I/F
14
106
CFUnit
AUnit
DUnit
LEAD3core

FIG. 2

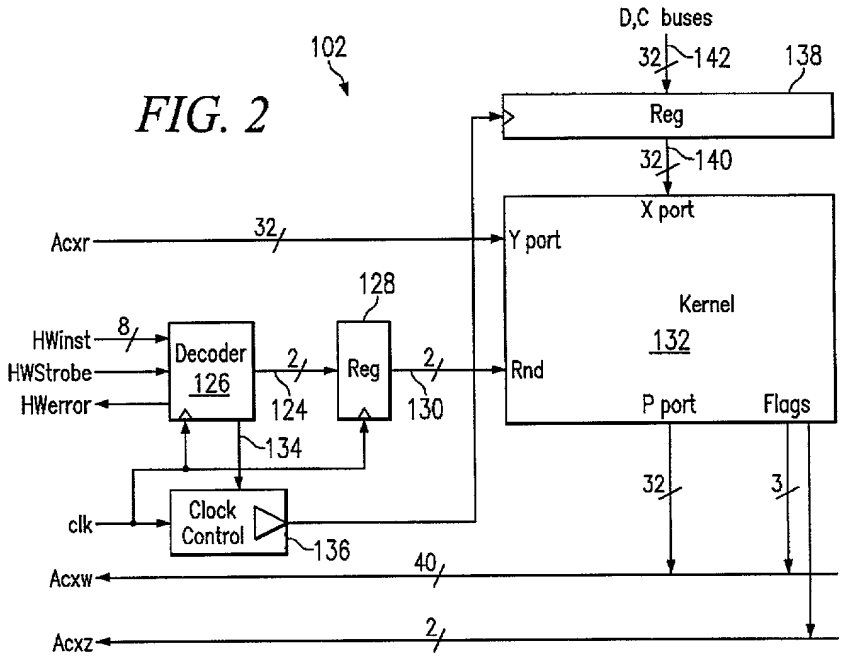

102
D,C buses
32
142
138
Reg
32
140
X port
Acxr
32
Y port
Kernel
132
128
HWinst
8
Decoder
126
2
Reg
2
Rnd
HWStrobe
HWerror
124
130
P port
Flags
134
32
3
clk
Clock
Control
136
40
Acxw
2
Acxz

FIG. 3

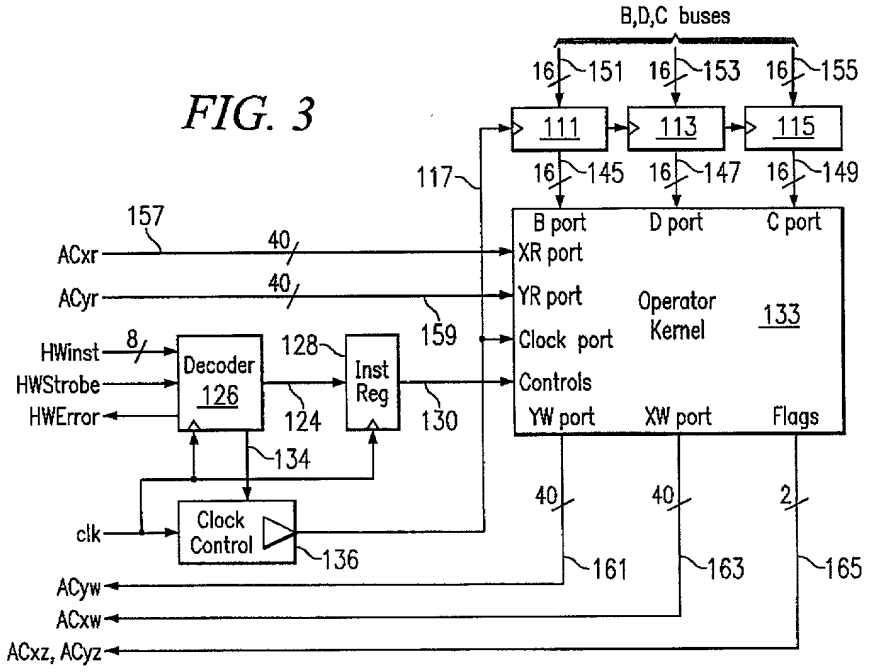

B,D,C buses
16
151
16
153
16
155
111
113
115
16
145
16
147
16
149
117
B port
D port
C port
157
ACxr
40
XR port
ACyr
40
YR port
Operator
Kernel
133
159
Clock port
HWinst
8
Decoder
126
128
Inst
Reg
Controls
HWStrobe
HWError
124
130
YW port
XW port
Flags
134
40
40
2
clk
Clock
Control
136
161
163
165
ACyw
ACxw
ACxz, ACyz

FIG. 4

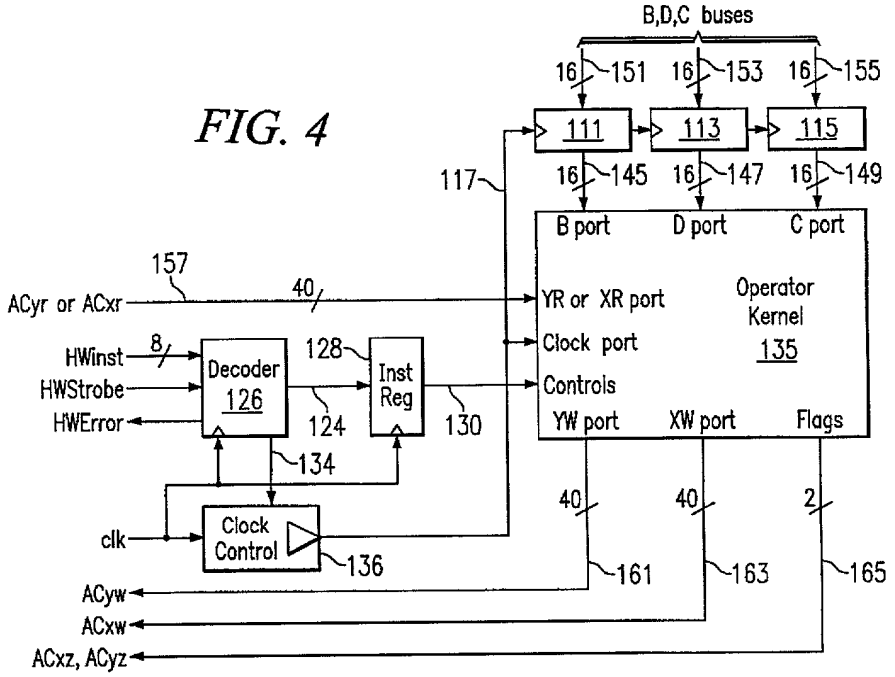

B,D,C buses
16
151
153
155
111
113
115
117
145
147
149
B port
D port
C port
157
ACyr or ACxr
40
YR or XR port
Operator Kernel
135
HWinst
8
Decoder 126
128
Inst Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
XW port
Flags
134
40
40
2
clk
Clock Control
136
161
163
165
ACyw
ACxw
ACxz, ACyz

FIG. 5

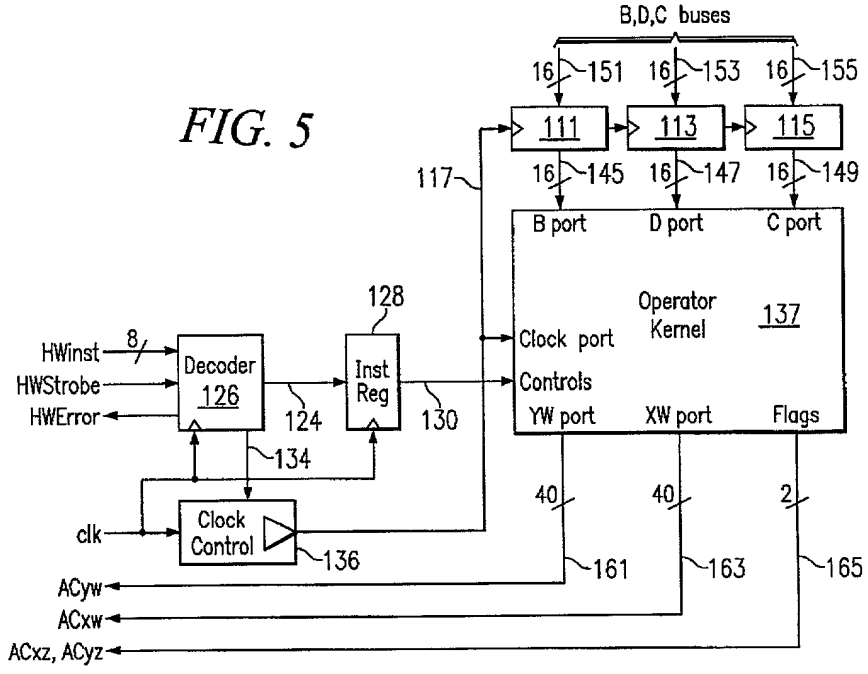

B,D,C buses
16
151
153
155
111
113
115
117
145
147
149
B port
D port
C port
128
Operator Kernel
137
HWinst
8
Decoder 126
Inst Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
XW port
Flags
134
40
40
2
clk
Clock Control
136
161
163
165
ACyw
ACxw
ACxz, ACyz

FIG. 6

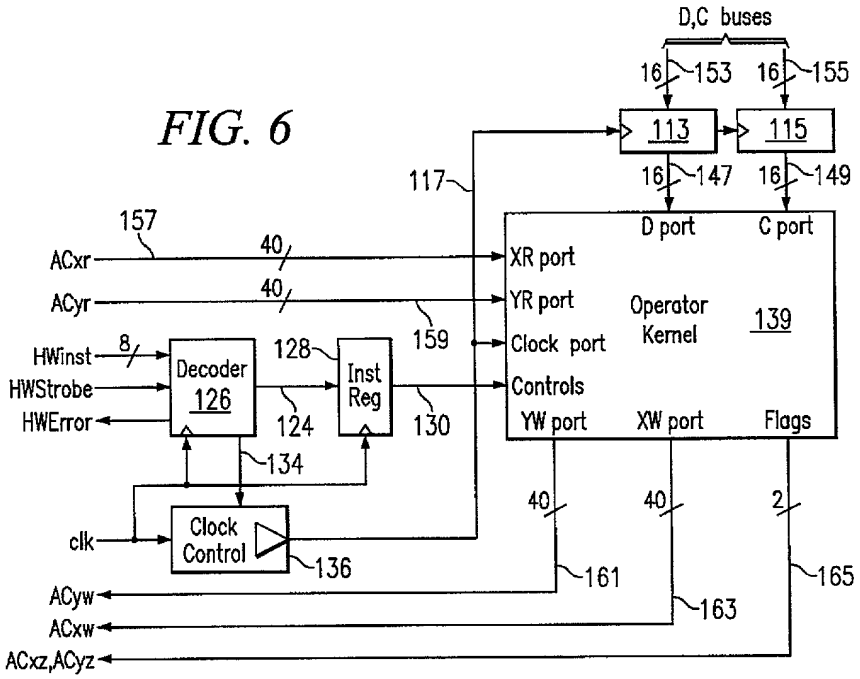

D,C buses
16
153
16
155
113
115
16
147
16
149
117
D port
C port
157
ACxr
40
XR port
ACyr
40
YR port
Operator
Kernel
139
159
HWinst
8
Decoder
126
128
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
XW port
Flags
134
40
40
2
clk
Clock
Control
136
161
165
ACyw
163
ACxw
ACxz,ACyz

FIG. 7

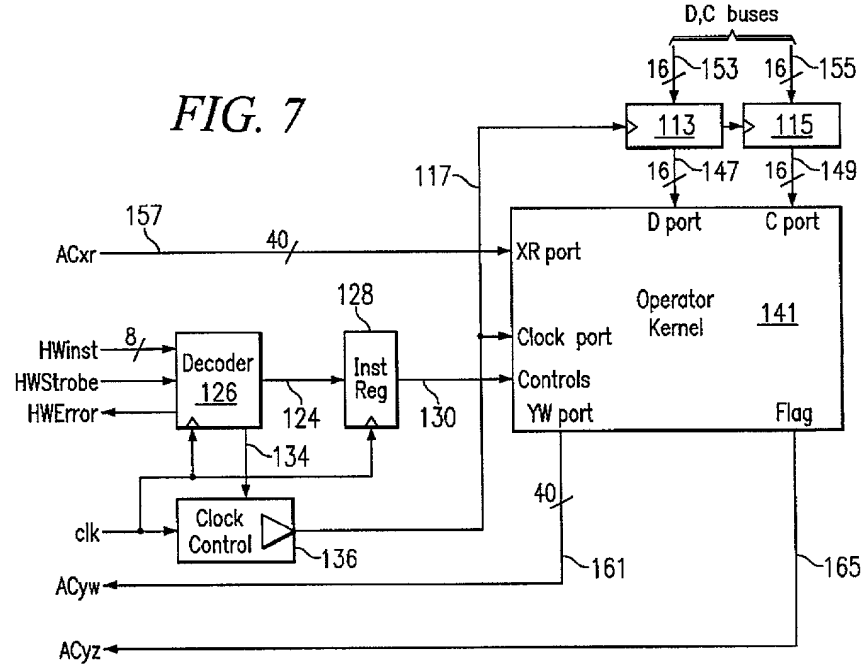

D,C buses
16
153
16
155
113
115
16
147
16
149
117
D port
C port
157
ACxr
40
XR port
Operator
Kernel
141
128
HWinst
8
Decoder
126
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 8

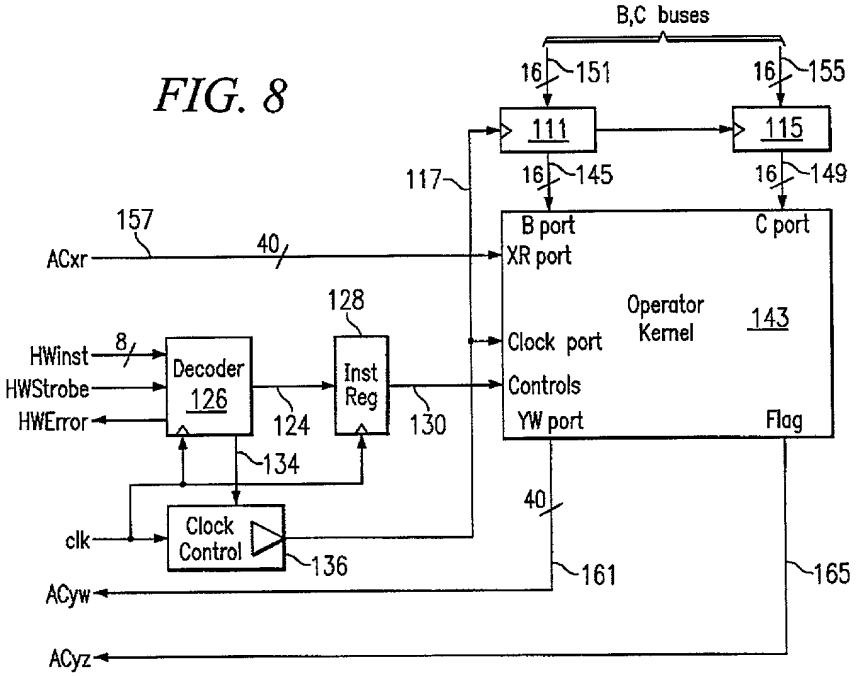

B,C buses
16
151
16
155
111
115
117
16
145
16
149
157
ACxr
40
B port
C port
XR port
128
Operator
Kernel
143
HWinst
8
Decoder
126
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 9

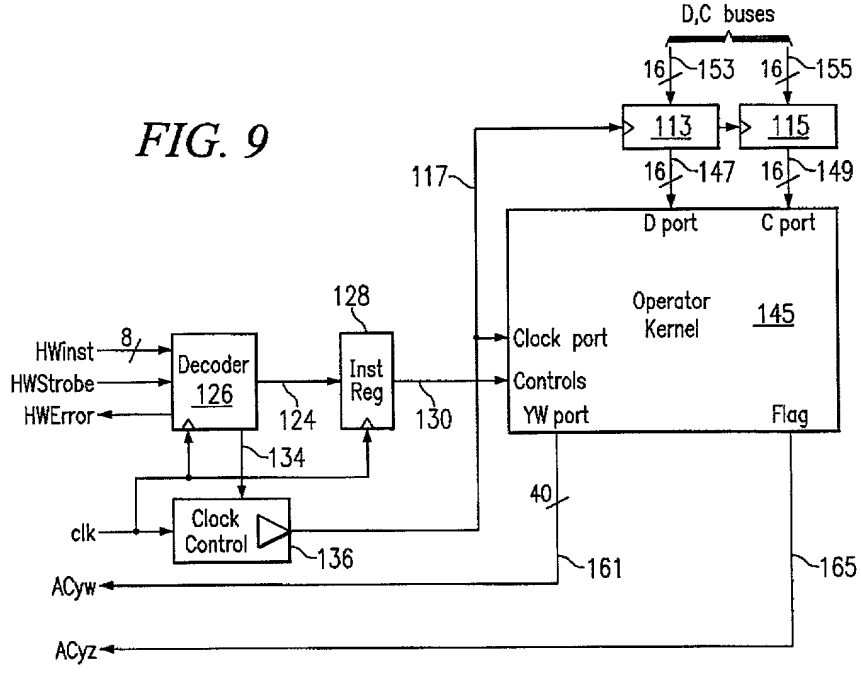

D,C buses
16
153
16
155
113
115
117
16
147
16
149
D port
C port
128
Operator
Kernel
145
HWinst
8
Decoder
126
Inst
Reg
Clock port
HWStrobe
Controls
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 10

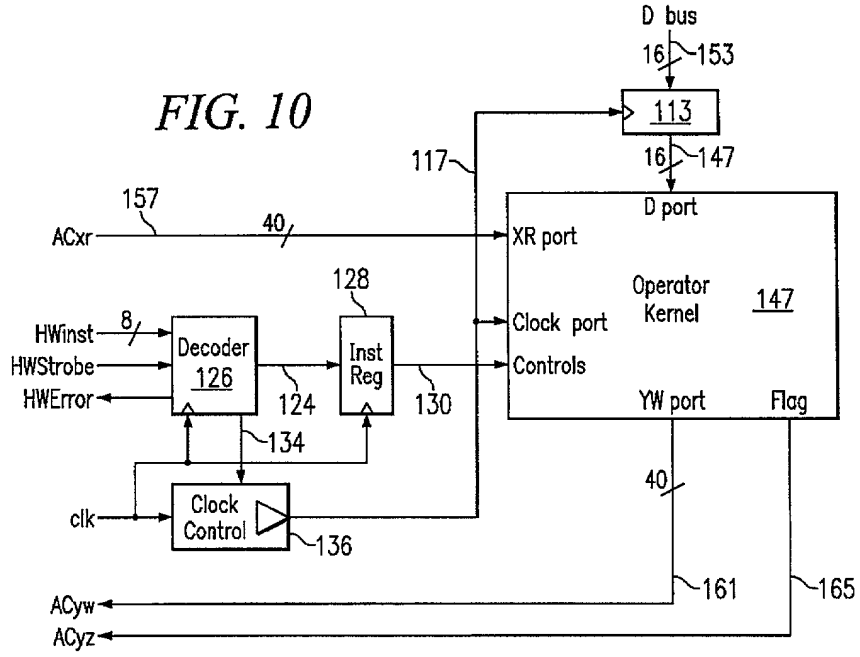

D bus
16
153
113
16
147
117
157
ACxr
40
D port
XR port
Operator
Kernel
147
128
HWinst
8
Decoder
126
Inst
Reg
Clock port
Controls
HWStrobe
HWError
124
130
YW port
Flag
134
40
clk
Clock
Control
136
161
165
ACyw
ACyz

FIG. 11

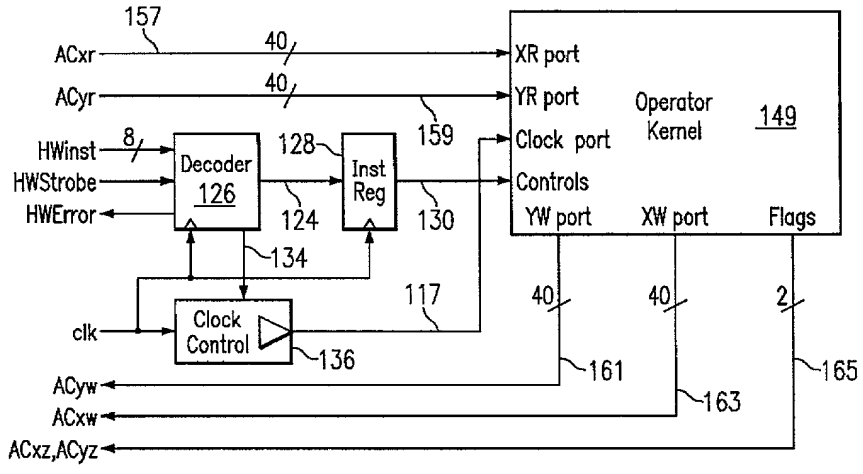
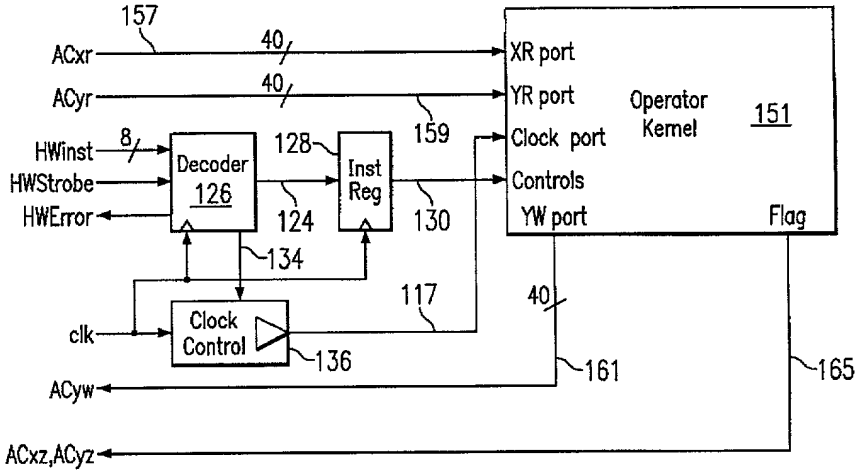

157
ACxr
40
ACyr
40
159
XR port
YR port
Operator
Kernel
149
HWinst
8
Decoder
126
128
Inst
Reg
Clock port
Controls
HWStrobe
HWError
124
130
YW port
XW port
Flags
134
117
40
40
2
clk
Clock
Control
136
161
163
165
ACyw
ACxw
ACxz,ACyz

FIG. 12


157
ACxr
40
ACyr
40
XR port
YR port
Clock port
Controls
YW port
Operator Kernel
151
159
HWinst
8
HWStrobe
HWError
Decoder 126
128
124
Inst Reg
130
134
117
40
clk
Clock Control
136
161
165
ACyw
ACxz,ACyz
Flag

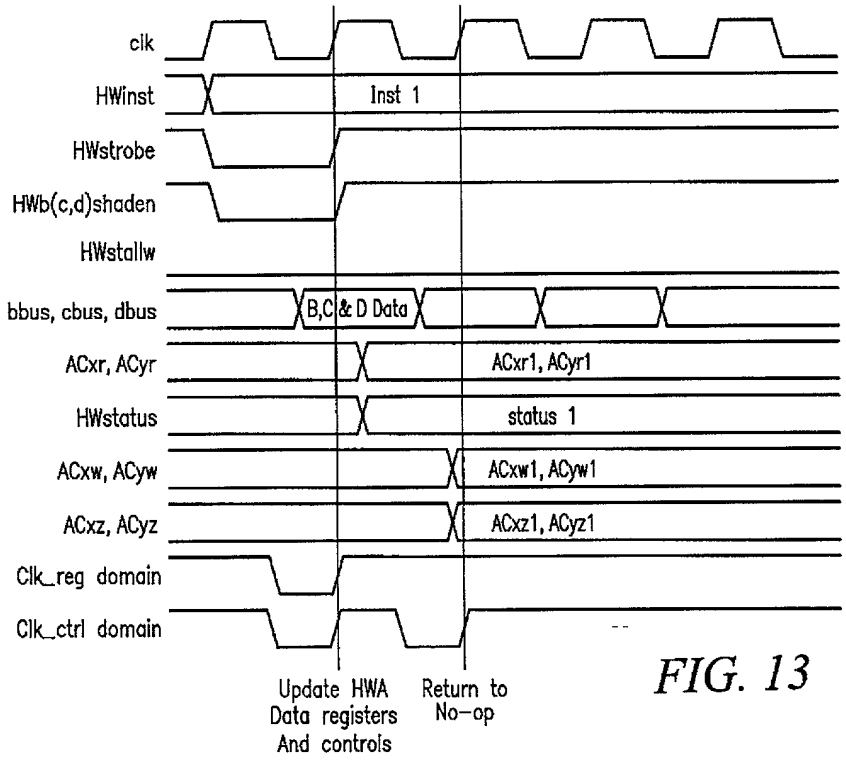

clk
HWinst
Inst 1
HWstrobe
HWb(c,d)shaden
HWstallw
bbus, cbus, dbus
B,C & D Data
ACxr, ACyr
ACxr1, ACyr1
HWstatus
status 1
ACxw, ACyw
ACxw1, ACyw1
ACxz, ACyz
ACxz1, ACyz1
Clk_reg domain
Clk_ctrl domain
Update HWA Data registers And controls
Return to No-op

FIG. 13

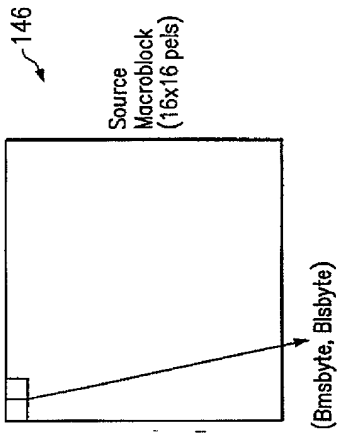


FIG. 15

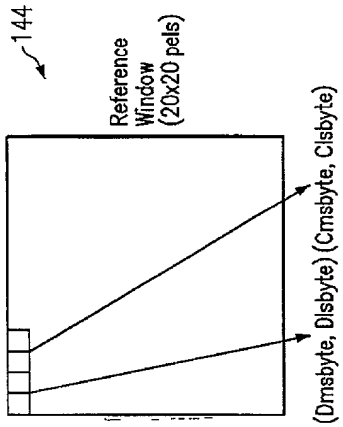


FIG. 14

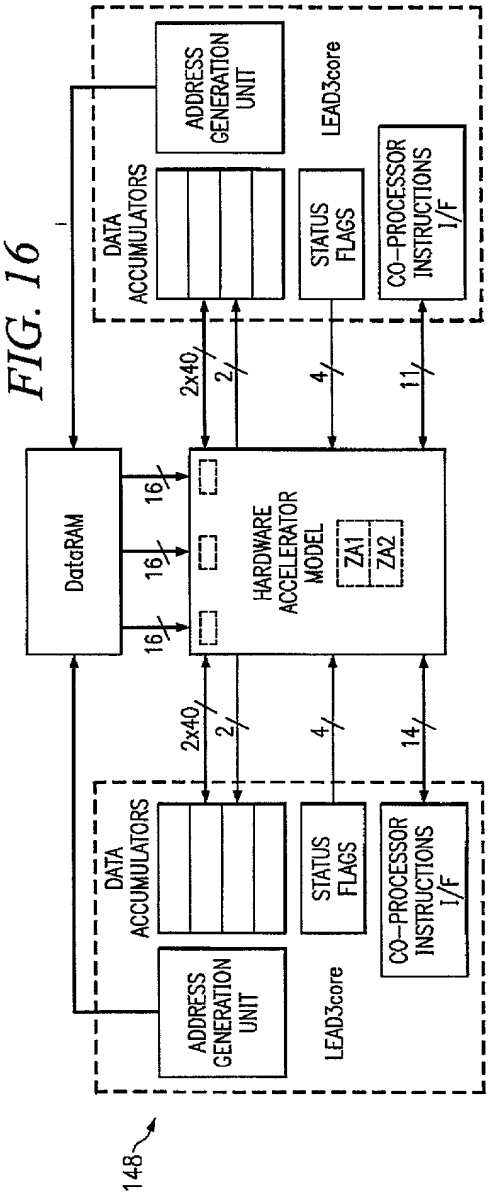


FIG. 16

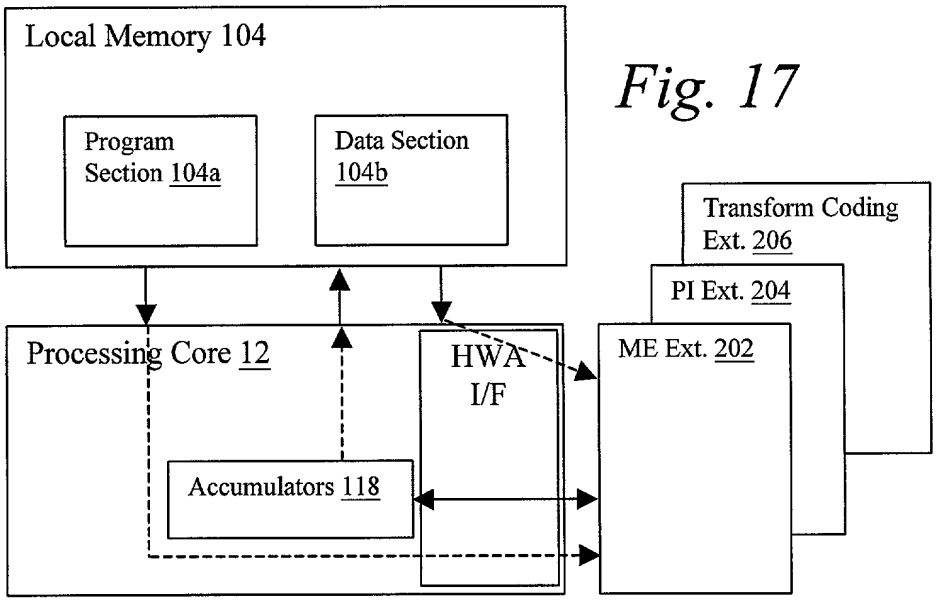
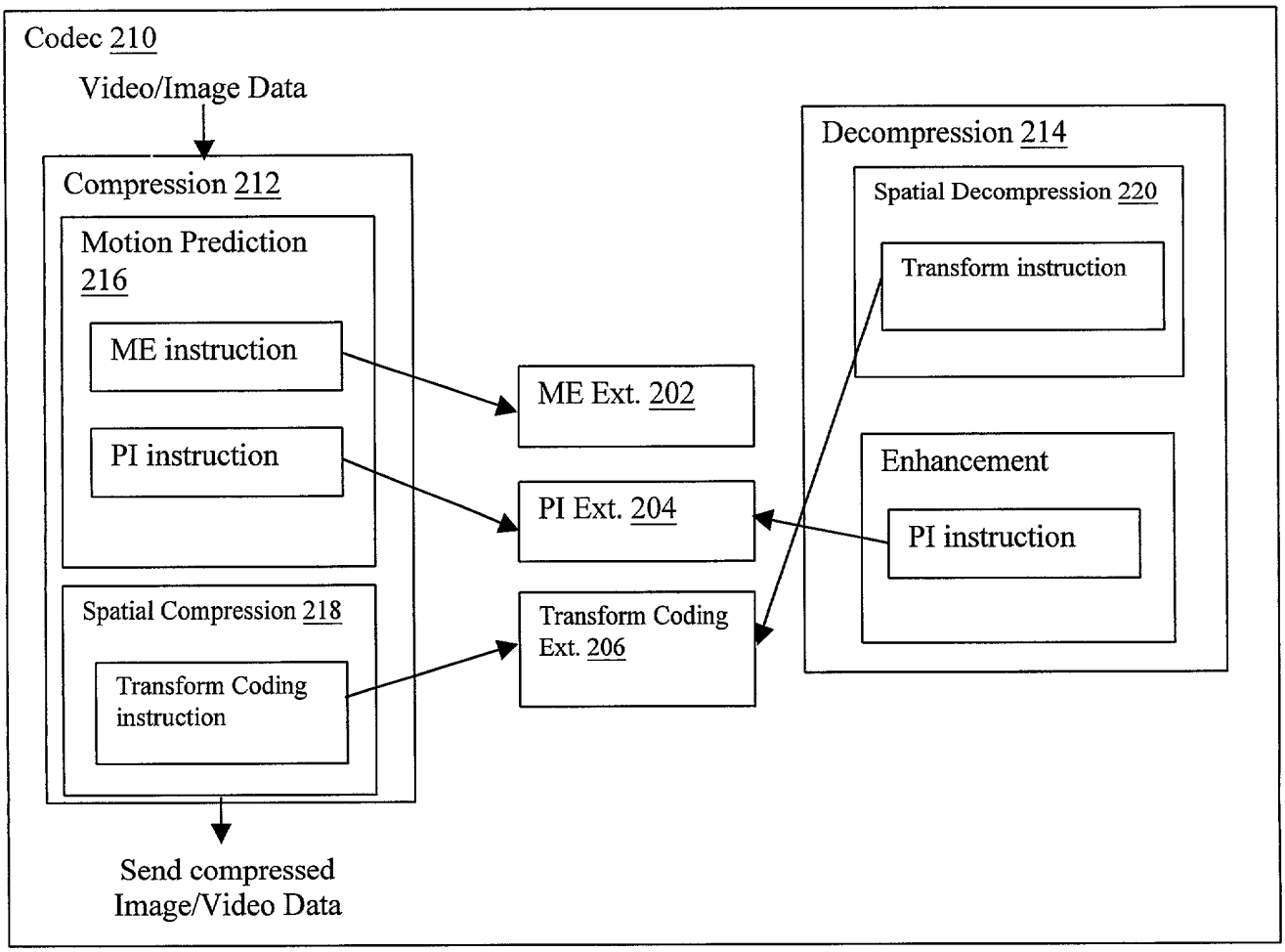

Local Memory 104
Program Section 104a
Data Section 104b
Transform Coding Ext. 206
PI Ext. 204
ME Ext. 202
Processing Core 12
HWA I/F
Accumulators 118

Fig. 17

Fig. 18


Codec 210
Video/Image Data
Compression 212
Motion Prediction 216
ME instruction
PI instruction
Spatial Compression 218
Transform Coding instruction
Send compressed Image/Video Data
ME Ext. 202
PI Ext. 204
Transform Coding Ext. 206
Decompression 214
Spatial Decompression 220
Transform instruction
Enhancement
PI instruction

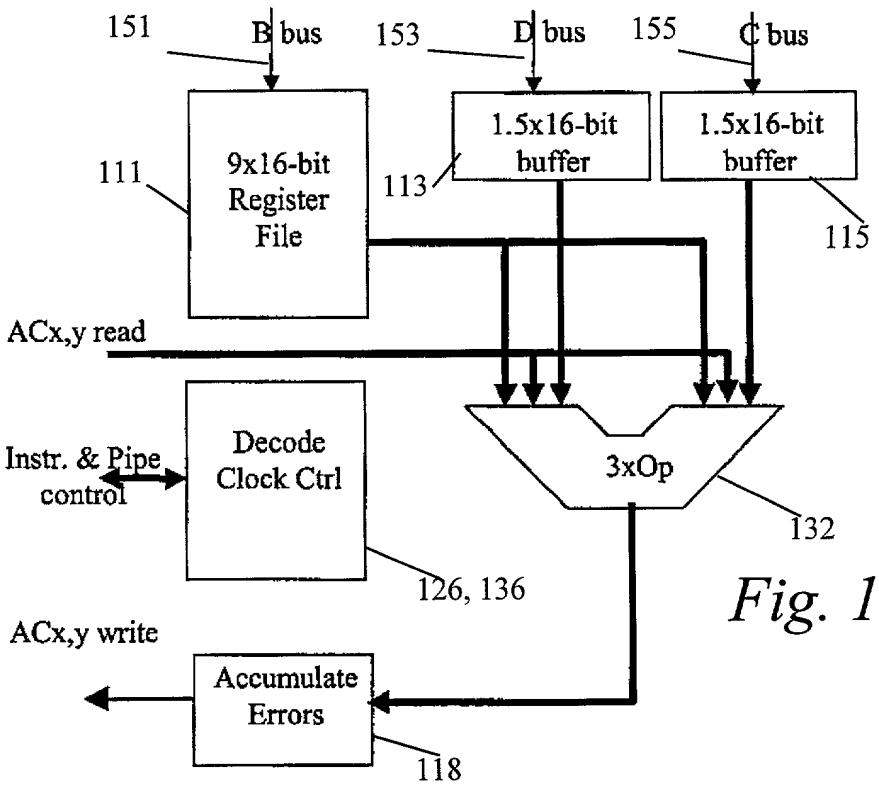


Fig. 19

Fig. 20

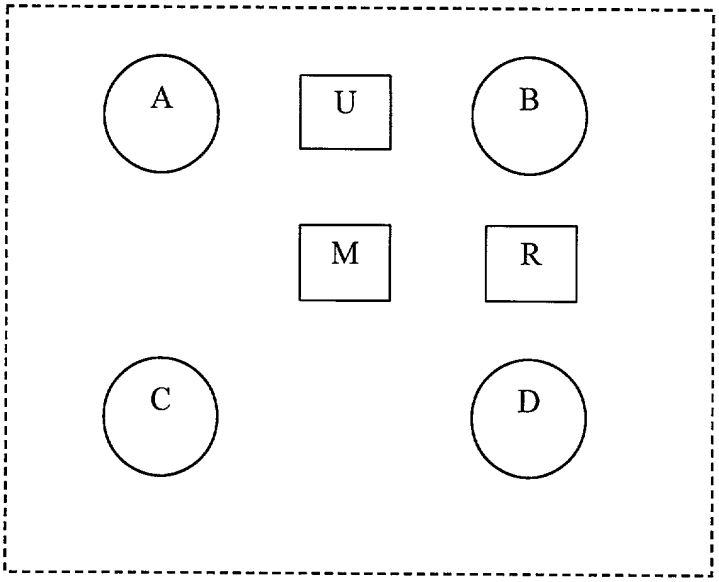
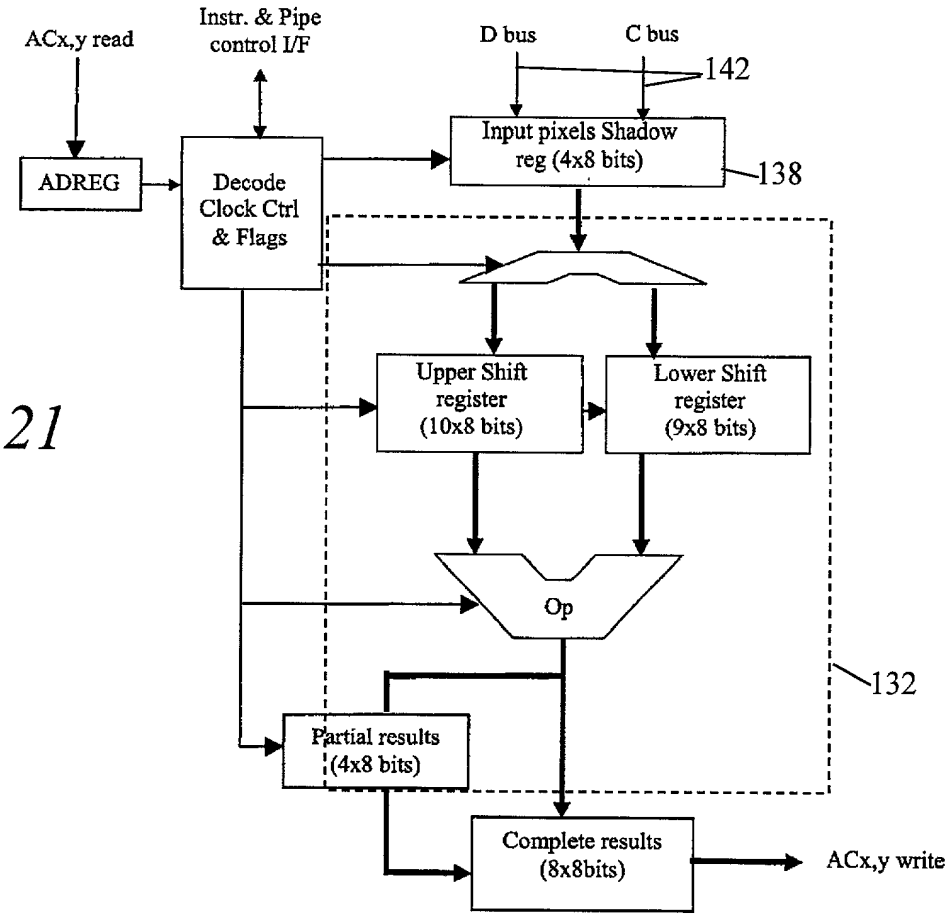

A
U
B
M
R
C
D

Fig. 21


ACx,y read
Instr. & Pipe control I/F
D bus
C bus
142
ADREG
Decode Clock Ctrl & Flags
Input pixels Shadow reg (4x8 bits)
138
Upper Shift register (10x8 bits)
Lower Shift register (9x8 bits)
Op
132
Partial results (4x8 bits)
Complete results (8x8bits)
ACx,y write

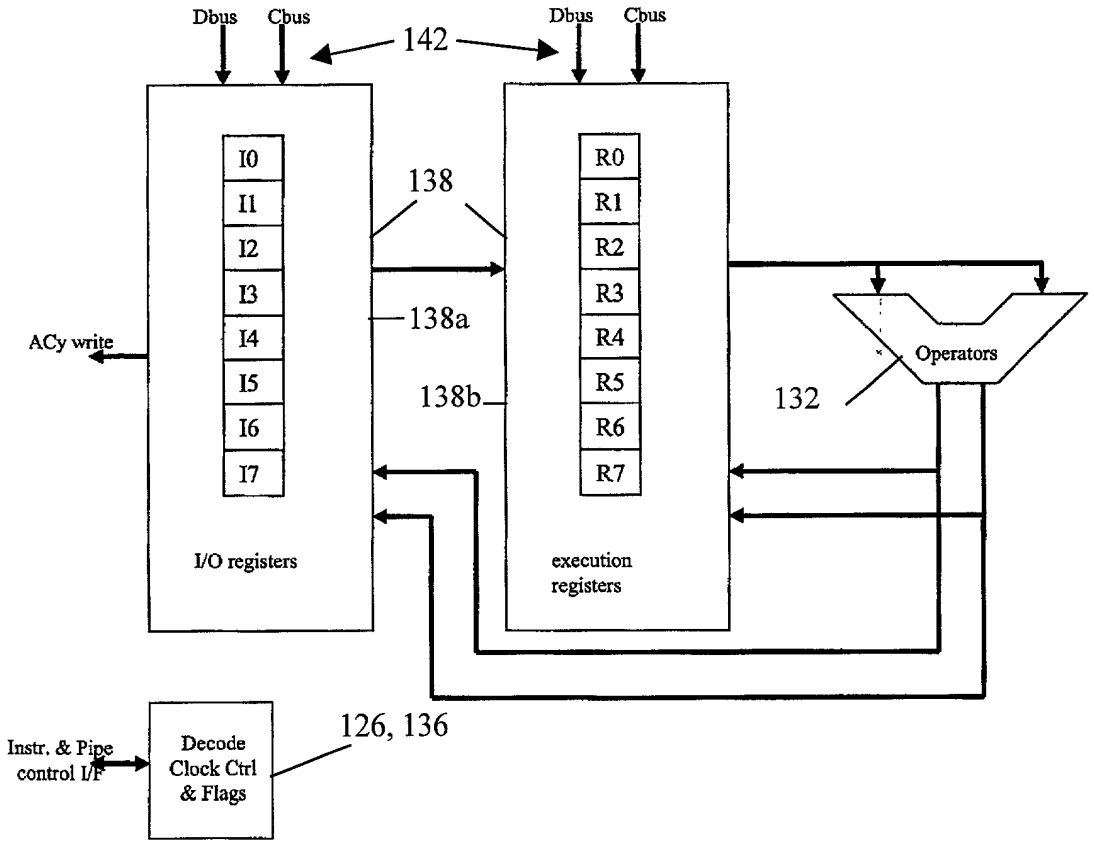

Dbus
Cbus
142
Dbus
Cbus
I0
I1
I2
I3
I4
I5
I6
I7
138
138a
138b
R0
R1
R2
R3
R4
R5
R6
R7
ACy write
Operators
132
I/O registers
execution registers
Instr. & Pipe control I/F
Decode Clock Ctrl & Flags
126, 136

Fig. 22

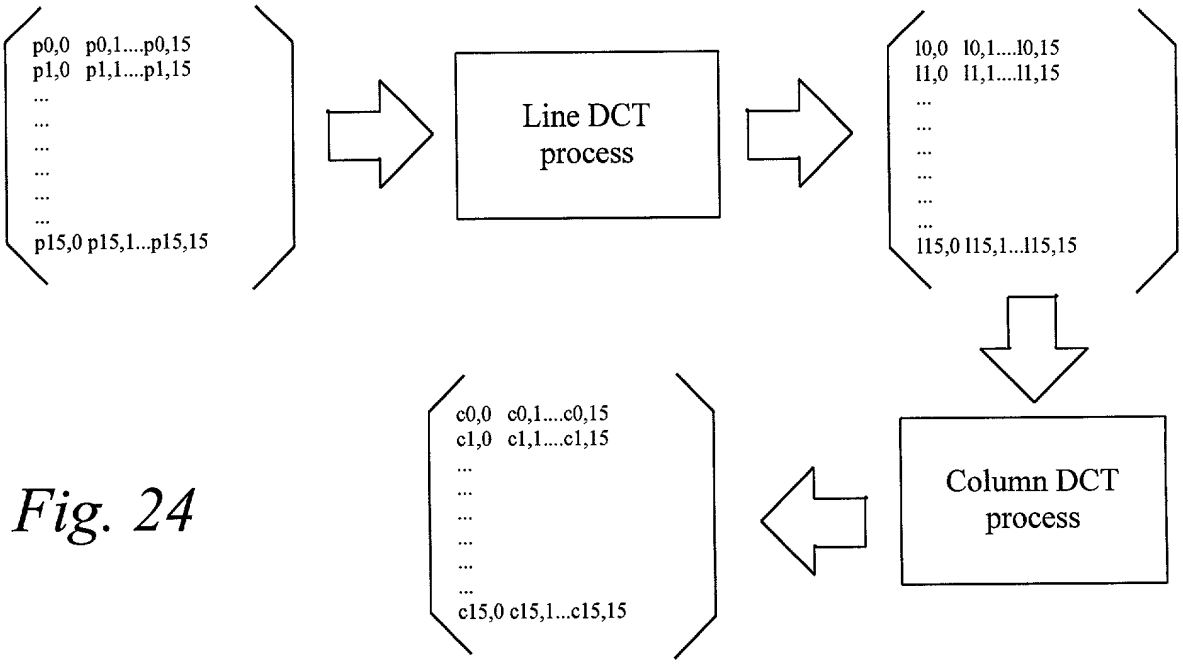

p0,0 p0,1....p0,15
p1,0 p1,1....p1,15
p15,0 p15,1...p15,15
Line DCT process
I0,0 I0,1....I0,15
I1,0 I1,1....I1,15
I15,0 I15,1...I15,15
Column DCT process
c0,0 c0,1....c0,15
c1,0 c1,1....c1,15
c15,0 c15,1...c15,15

Fig. 24

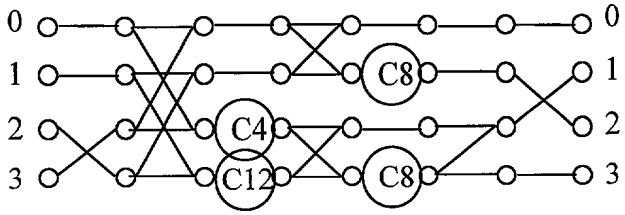


Fig. 23a

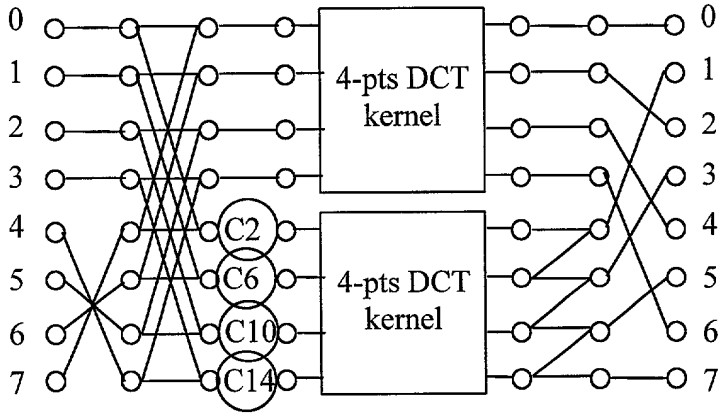


Fig. 23b

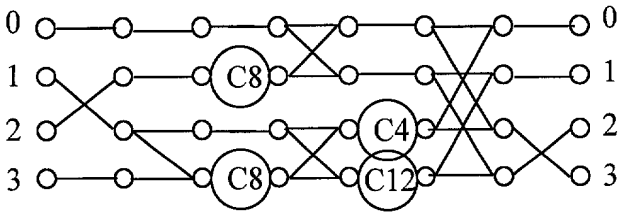


Fig. 23c

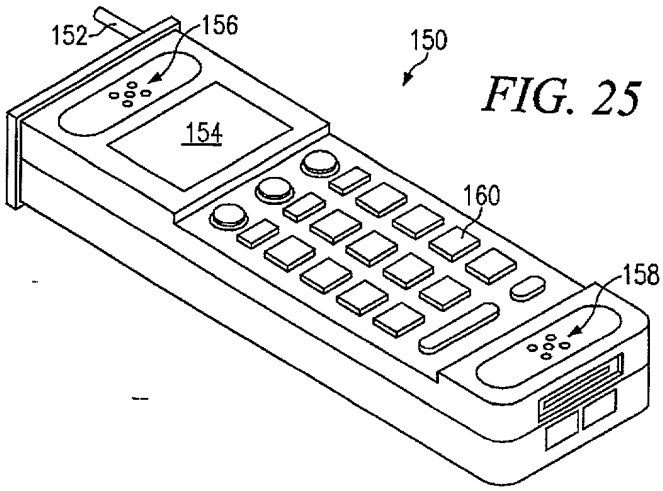

152
156
150
154
160
158

FIG. 25

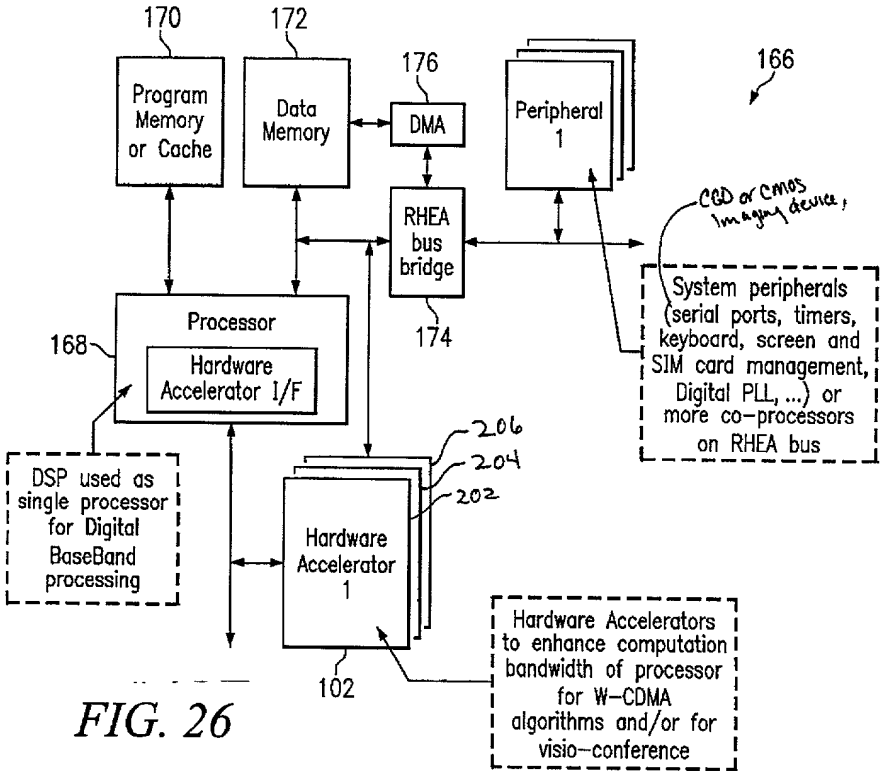

170
172
176
166
Program Memory or Cache
Data Memory
DMA
Peripheral 1
RHEA bus bridge
CCD or CMOS imaging device
System peripherals (serial ports, timers, keyboard, screen and SIM card management, Digital PLL, ...) or more co-processors on RHEA bus
174
168
Processor
Hardware Accelerator I/F
206
204
202
DSP used as single processor for Digital BaseBand processing
Hardware Accelerator 1
102
Hardware Accelerators to enhance computation bandwidth of processor for W-CDMA algorithms and/or for visio-conference

FIG. 26